

Remarks

The Examiner has rejected applicants' claims 38-43 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner has argued that these claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Particularly, the Examiner has argued as follows:

"The specification does not describe an first encoder for encoding a first digital information and output parallel data of L bits and first converting for converting into parallel data of L bits into the first parallel data of N bits and an error correcting unit for adding the error correcting coded into the first parallel data as being recited in claims 38-43. It is noted that the specification teaches only the MUSE signal is processed into parallel data. See Fig.12."

Applicants respectfully disagree with the Examiner's argument. More particularly, as can be seen in FIG. 12 of applicants' drawings, the data line from the A/D converter 12, the data line from the compressor 14 and the data line from the converter buffer 16 each have a slash line through the line and a number adjacent the slash line. As is customary in electrical circuit diagrams, a slash line through a data line is used to indicate that the line is actually a plurality of parallel data lines and the number adjacent the slash line indicates the number of parallel lines. Attached is a copy of a "22C: 122, Lecture Notes, Lecture 3, Fall 1999", by Douglas W. Jones, University of Iowa Department of Computer Science, in which on page 5, this use of a slash line and an adjacent number to indicate a number of parallel data lines is confirmed by the following statement:

"When drawing a circuit diagram with many parallel data lines, it is common to draw one line and then annotate it saying this

is one of many by putting a slash line with the number of lines indicated." (Emphasis Added).

Accordingly, it would be understood by one of skill in the art from FIG. 12 of applicants' drawings that the A/D converter 12 converts the Y signal into 8-bit parallel data (indicated by the slash line and the number 8), the compressor 14 converts the Y 8-bit parallel data into Y 4-bit parallel data (indicated by the slash line and the number 4) and the converter buffer 16 converts the Y 4-bit parallel data into Y 8-bit parallel data (indicated by the slash line and the number 8). The latter Y 8-bit parallel data is then conveyed to the error correction encoders ECC 54-1, 54-2 and 54-3. The compressor 14, the converter buffer 16 and the error correction units ECC 54-1, 54-2 and 54-3 in conjunction with the slash lines and adjacent numbers in the lines from these units shown in FIG. 12, as well as the description in applicants' specification of recording the Y signal on page 14, line 19, through page 15, line 22, page 19, line 3 through page 20, line 22, page 30, lines 20-26, and page 31, line 24 through page 32, line 2, thus provide support for the first encoder, first converter and error correction unit recited in applicant's independent apparatus claim 38 and the corresponding encoding, converting and error check code adding method steps in applicants' independent method claim 43.

In summary, therefore, it is submitted that applicants' claims 38-43 are supported by an enabling disclosure. Such claims, therefore, meet the requirements of 35 USC § 112, first paragraph.


In view of the above, it is submitted that applicants' claims meet all statutory requirements. Accordingly, reconsideration of the claims and passage of same and this application to issue is respectfully requested.

Accompanying this Amendment is a Request for an Interview requesting that applicants' undersigned attorney be permitted to conduct an interview with the Examiner to discuss the subject Response and the application, in the event the Examiner is still not disposed to allow the application.

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Respectfully submitted,


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